NAME _____

OPEN BOOK/OPEN NOTES:

1. (20 points) Interrupts
a. Explain the advantage of using interrupts for handling I/O instead
of using status polling.

b. Explain how the IRET instruction differs from the RET instruction
and explain where you would use each of them?

2. (20 points) Combinational and Sequential Logic
a. Put an X by the logic devices that would NEVER be present in a
combinational logic circuit.

     (1) __ NAND   (4) __ Tri-State Driver
     (2) __ NOR   (5) __ J-K Flip-Flop
     (3) __ R-S Flip-Flop

b. Explain why it is harder to test a sequential logic circuit than to
test a combinational logic circuit and what you need to do.

3. (20 points) CPU and Bus Architecture
a. Explain a situation where the CPU would not be driving the address bus
during a bus cycle to/from memory.

b. Why is there a problem writing a 16 bit value to the PIT chip and what do
you need to do in your code?

4. (10 points) Address Decoding
Given the following logic to control the enable input on a memory chip
with a processor that has a 16 bit address bus and no M/IO# signal,
what range of addresses will select a memory location in this chip?

a. HEX ADDRESS RANGE: 0x_____ to 0x_____

A15

A14

A13

A12

A11

CE

A10
A09
A08
A07
A06
A05
A04
A03
A02
A01
A00
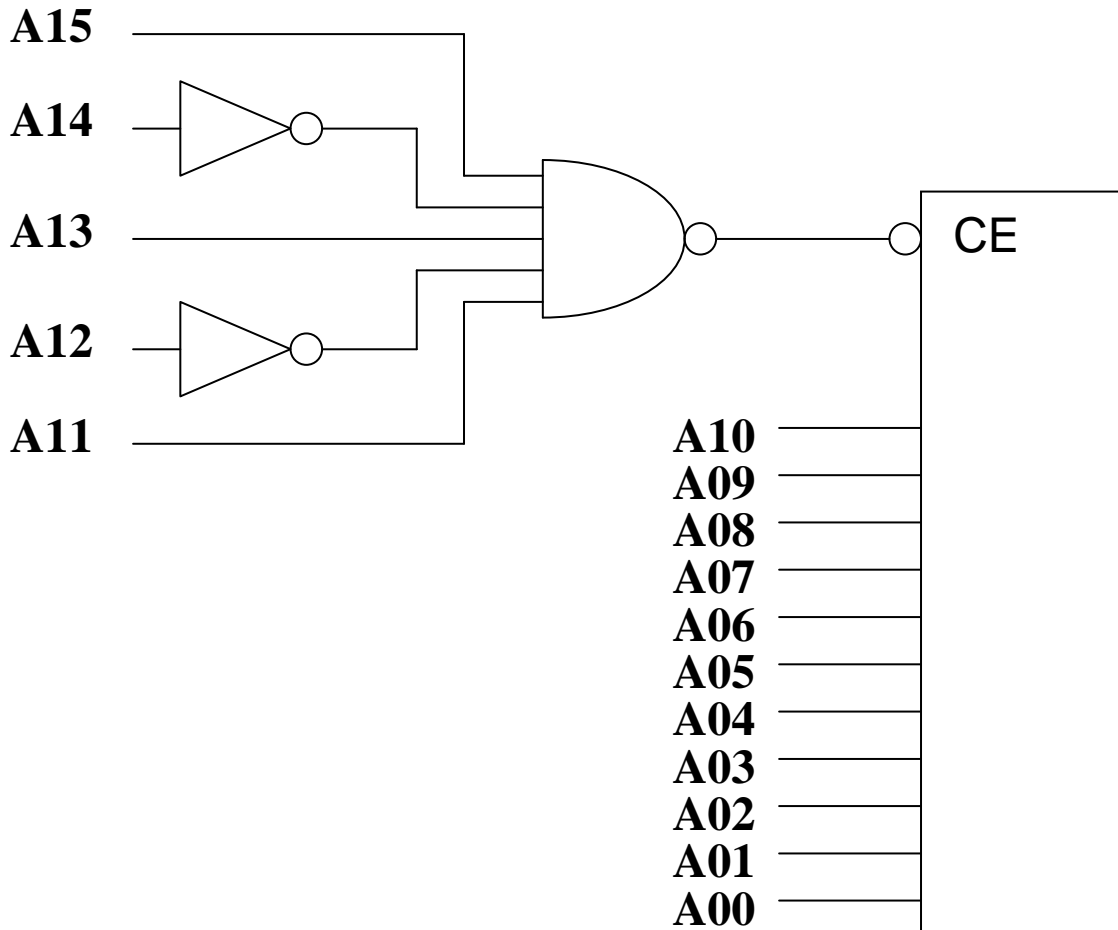
b. Assuming that there are 16 signals in the address bus (A15-A00), are
there reflections of this chip in more than one range of addresses?

CHECK ONE: YES _____ NO _____

**If yes, how many reflections and for which address ranges?**

5. (30 points)
Develop a simplified logic equation for segment a of a 7 segment display
and draw the logic diagram using standard logic symbols.

Here is a picture of the segments and the decimal digit displays needed.
The display is driven by BCD code DCBA and values 10-15 are don't care.
$(D = 2^3, C = 2^2, B = 2^1, and A = 2^0)$.
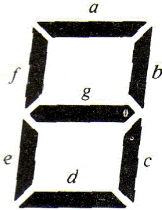
(a) Segment identification
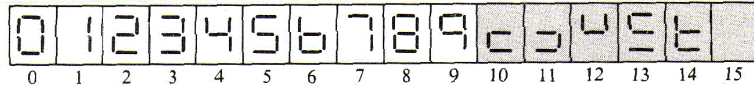
(b) Decimal number with typical display

Fig. 7-10 Seven-segment display

D	C	B	A	Y
0	0	0	0	_
0	0	0	1	_
0	0	1	0	_
0	0	1	1	_
0	1	0	0	_
0	1	0	1	_
0	1	1	0	_
0	1	1	1	_
1	0	0	0	_
1	0	0	1	_
1	0	1	0	_
1	0	1	1	_
1	1	0	0	_
1	1	0	1	_
1	1	1	0	_
1	1	1	1	_

There is a blank four input Karnaugh map on the next page.

Label the rows and columns properly. Fill in all cells with 0, 1, or X.
Circle the optimal patterns to derive a **product of sums** logic equation
(no further factoring required) and draw the logic diagram.

Logic Equation:

Segment a =

Logic Diagram:

EXAM #1 SOLUTIONS:

1.
a. Status polling ties up the processor in a loop checking the state of a status bit from the device. Using an interrupt when the status bit changes state lets the processor do useful work while it's waiting for the I/O device to become ready.

b. The IRET instruction pops the code segment register and the eflags register in addition to the eip register. The RET instruction pops only the eip register. IRET is used at the end of an interrupt service routine. RET is used at the end of a function called by software.

2. a. Put an X by the logic devices that would NEVER be present in a combinational logic circuit.

        (1)   __ NAND   (4) __ Tri-State Driver
        (2)   __ NOR   (5) X   J-K Flip-Flop
        (3)   X   R-S Flip-Flop

b. It is harder to test a sequential logic circuit than to test a combinational logic circuit because there is memory inside. You need to test the logic with all possible input values together with each possible internal state based on the values stored in the memory.

3. a. The CPU would not be driving the address bus during a Direct Memory Access bus cycle. The DMA controller would be driving it. The CPU might also not be driving the address bus during a DRAM refresh cycle or while another CPU was driving the bus to access shared memory.

b. The PIT has only 8 data bus lines so it can only accept 8 bits of data in one bus cycle. You must use two instructions to write 2 bytes.

4. Address Decoding

a. HEX ADDRESS RANGE: 0xA800 to 0xAFFF
    A15 = 1
    A14 = 0
    A13 = 1
    A12 = 0   = Hex A

    A11 = 1
    A10 goes to chip
    A09 goes to chip
    A08 goes to chip   = Hex 8 – F based on A10, A09, and A08

b. No reflections. All 16 address lines are used to decode a location in the memory chip. This is an example of full address decoding. If an address line had been left out of the chip enable logic computation, there would be an address reflection at values where that address bit is what differentiates between the addresses.

5. Segment a of 7 segment display:
For a product of sums solution, we concentrate on the Y = 0 rows.
D C B A   Y

0 0 0 0   1
0 0 0 1   0
0 0 1 0   1
0 0 1 1   1
0 1 0 0   0
0 1 0 1   1
0 1 1 0   0
0 1 1 1   1
1 0 0 0   1
1 0 0 1   1
1 0 1 0   x
1 0 1 1   x
1 1 0 0   x
1 1 0 1   x
1 1 1 0   x
1 1 1 1   x

	$\overline{C}\ \overline{D}$	$\overline{C}\ D$	$C\ D$	$C\ \overline{D}$
$\overline{A}\ \overline{B}$	1	1	X	0
$\overline{A}\ B$	1	X	X	0
$A\ B$	1	X	X	1
$A\ \overline{B}$	0	1	X	1

Logic Equation:

Segment a = (D + C + B + $\overline{A}$) * ($\overline{C}$ + A)